| L Number | Hits | Search Text | DB | Time stamp |
|---|---|---|---|---|
| 1 | 232 | 345/698.ccls. | USPAT | 2003/12/04 18:26 |
| 2 | 102 | 345/698.ccls. and (lcd or liquid NEAR1 crystal) | USPAT | 2003/12/04 18:31 |
| 3 | 44 | (345/698.ccls. and (lcd or liquid NEAR1 crystal)) and sampl$3 | USPAT | 2003/12/04 18:48 |
| 4 | 8 | ("4990904" \| "5351064" \| "5448260" \| "5592194" \| "5627559" \| "5748175" \| "5771040" \| "5844539").PN. | USPAT | 2003/12/04 18:44 |
| 5 | 2 | ("4990904" \| "5111190").PN. | USPAT | 2003/12/04 18:46 |
| 6 | 2 | 5771040.URPN. | USPAT | 2003/12/04 18:46 |
| 7 | 3736 | 345/87-103.ccls. | USPAT | 2003/12/04 18:48 |
| 8 | 50323 | tim$3 NEAR2 (generat$3 or control$4) WITH (detect$3 or sens$3 or measur$3) | USPAT | 2003/12/04 18:49 |
| 9 | 109 | 345/87-103.ccls. and (tim$3 NEAR2 (generat$3 or control$4) WITH (detect$3 or sens$3 or measur$3)) | USPAT | 2003/12/04 18:50 |
| 10 | 27 | (345/87-103.ccls. and (tim$3 NEAR2 (generat$3 or control$4) WITH (detect$3 or sens$3 or measur$3))) and sampl$3 and reset$3 | USPAT | 2003/12/04 19:08 |
| 11 | 10 | ("4376268" \| "4385395" \| "4617594" \| "5396295" \| "5459419" \| "5528309" \| "5594763" \| "5668594" \| "5731843" \| "6133900").PN. | USPAT | 2003/12/04 18:56 |
| 12 | 7 | ("4393379" \| "4455576" \| "4635127" \| "4694348" \| "4694349" \| "4789899" \| "4792857").PN. | USPAT | 2003/12/04 19:06 |
| 13 | 13 | 5057928.URPN. | USPAT | 2003/12/04 19:07 |
| 14 | 883 | 345/99-100.ccls. | USPAT | 2003/12/04 19:08 |
| 15 | 298 | 345/99-100.ccls. and sampl$3 WITH (tim$3 or clock) | USPAT | 2003/12/04 19:11 |
| 16 | 289 | (345/99-100.ccls. and sampl$3 WITH (tim$3 or clock)) not ((345/87-103.ccls. and (tim$3 NEAR2 (generat$3 or control$4) WITH (detect$3 or sens$3 or measur$3))) and sampl$3 and reset$3) | USPAT | 2003/12/04 19:12 |
| 17 | 256 | ((345/99-100.ccls. and sampl$3 WITH (tim$3 or clock)) not ((345/87-103.ccls. and (tim$3 NEAR2 (generat$3 or control$4) WITH (detect$3 or sens$3 or measur$3))) and sampl$3 and reset$3)) and (sens$3 or detect$3 or measur$3 or receiv$3) | USPAT | 2003/12/04 19:24 |
| 18 | 4 | ("5053862" \| "6181330" \| "6348931" \| "6392642").PN. | USPAT | 2003/12/04 19:16 |
| 19 | 9 | ("5031118" \| "5406308" \| "5592194" \| "5633655" \| "5654738" \| "5889927" \| "5929924" \| "6037925" \| "6078317").PN. | USPAT | 2003/12/04 19:18 |
| 20 | 2 | ("4990902" \| "5031118").PN. | USPAT | 2003/12/04 19:21 |
| 21 | 33 | 5406308.URPN. | USPAT | 2003/12/04 19:21 |
| 22 | 78 | ((345/99-100.ccls. and sampl$3 WITH (tim$3 or clock)) not ((345/87-103.ccls. and (tim$3 NEAR2 (generat$3 or control$4) WITH (detect$3 or sens$3 or measur$3))) and sampl$3 and reset$3)) and (sens$3 or detect$3 or receiv$3 or input$5) SAME (reset$3 or Hset or yset) | USPAT | 2003/12/04 19:30 |
| 23 | 3736 | 345/87-103.ccls. | USPAT | 2003/12/04 19:31 |
| 24 | 6340 | (reset$3 or chang$3 or vary$4) NEAR5 sampl$3 NEAR3 (tim$3 or clock) | USPAT | 2003/12/04 19:31 |

means). And, the C-V characteristic of the memory means may be asymmetric when the liquid crystal has an asymmetric characteristic.

In addition to the seventh aspect, a tenth aspect of the liquid crystal display device of the invention is where the memory means has a first ferroelectric capacitor having a first polarity and a second ferroelectric capacitor having a second polarity which is converse to the first polarity connected in parallel with the first ferroelectric capacitor.

In addition to the seventh aspect, an eleventh aspect of the liquid crystal display device of the invention is where the memory means has a capacitor which is formed of a ferroelectric substance movably inserted between a pair of electrodes, and overlap of the electrodes and the dielectric substance is variable corresponding to the data signal. The dielectric substance includes both a paraelectric substance and a ferroelectric substance.

A twelfth aspect of the liquid crystal display device of the invention comprises a liquid crystal layer intervened between a first electrode and a second electrode; a voltage applying means for applying an AC voltage to the first electrode or the second electrode; a first polar memory element which is connected to the second electrode and has an asymmetrical capacitance variance with respect to a voltage applied; a second polar memory element which is connected to the second electrode in parallel with and having a reverse polarity from the first polar memory element and has an asymmetrical capacitance variance with respect to a voltage applied; and a signal applying means for applying a data signal to the first and second polar memory elements.

A thirteenth aspect of the invention comprises an array substrate which has a plurality of pixel electrodes arranged in a matrix; an opposed substrate having an opposed electrode which is opposed with the array substrate through a liquid crystal layer; a memory means which is connected in series with the respective pixel electrodes and holds the data signal as a capacitance variable corresponding to the data signal; and means for applying an AC voltage to the opposed electrode. The memory means is provided for every pixel and holds the data signal corresponding to the pixel. On the other hand, since the AC voltage is applied as a signal common to the opposed electrode (formed over the plurality of pixels), the structure of the liquid crystal display device can be simplified.

When the liquid crystal capacitance asymmetrically depends on the positive or negative of a voltage to be applied, a memory capacitative element having an asymmetrical capacitance changing characteristic with respect to the voltage to be applied is used. And, the AC voltage to be applied to the second electrode is also accordingly a symmetrical.

Examples of the polar memory element include an element having the above-described multilayered structure of a metal electrode, a ferroelectric layer and a semiconductor layer; an element having the structure which has an insulator between a ferroelectric layer and a semiconductor layer, and an element having the structure which has a metal electrode and an insulator between a ferroelectric layer and a semiconductor layer.

The signal applying means applies, for example, data signals mutually having a reverse polarity to the first and second polar memory elements.

With the liquid crystal display device of the invention, a data signal as image information for displaying halftone on each pixel can be stored in the pixels of the liquid crystal display device. As a result, the frequent refresh of pixels can be omitted during the display of a still image. Therefore, power consumption can be reduced substantially.

And, with the liquid crystal display device of the invention, whatever data signal is held by the memory element, a voltage corresponding to the data signal can be applied in an analog fashion to the liquid crystal layer. As a result, it is possible to store the data signal of halftone and to display halftone in each pixels, and a liquid crystal display device having very high image quality can be achieved.

FIG. 9A and FIG. 9E are diagrams for describing the basic structure of a pixel in the liquid crystal display device of the invention. A liquid crystal layer **2** is connected in series with a memory unit **30** for holding a data signal. In FIG. 9E, the liquid crystal layer 2 is connected in series with the memory unit **30** which holds the data signal as a capacitance variable corresponding to a level of the data signal. In FIG. 9A, the memory unit **30** comprises memory elements *6a*, *6b*. And, terminals *30b*, *30c* are generally kept at substantially the same potential to each other.

The memory unit **30** has a nearly symmetrical C-V characteristic. With the liquid crystal display device of the invention, to achieve gradational display, the memory unit **30** is formed of a memory element having the capacitance variable corresponding to the data signal, such as a variable capacitance element (variable capacitor). FIG. 9A shows one example of the structure of the memory unit **30**. The memory unit **30** is formed of a pair of ferroelectric capacitors having a different polarity connected in parallel.

FIG. 9B and FIG. 9C are diagrams for describing the structure of the memory element **6**. The memory elements *6a*, *6b* are formed of a multilayered structure (MFS structure) of a metal electrode **7**, a ferroelectric layer **8** and a semiconductor layer **9** as shown in FIG. 9C. And, the memory elements *6a*, *6b* may have an MFIS structure with an insulator intervened between the ferroelectric layer **8** and the semiconductor layer **9** or an MFMIS structure with the second metal electrode and the insulator intervened between the ferroelectric layer **8** and the semiconductor layer **9**.

And, the memory element **6** may be formed of a variable capacitor. For example, an electric field produced by electrodes which are mutually opposed with a ferroelectric substance movably intervened therebetween and the overlap of the dielectric substance are varied to vary the capacitance. The dielectric substance includes both a paraelectric substance and a ferroelectric substance.

FIG. 9D shows a capacitance-voltage characteristic (C-V characteristic) of the memory element having the structure of FIG. 9C using amorphous silicon as the semiconductor layer **9**. In a general metal-insulator-semiconductor structure (MIS structure), when a positive voltage is applied to the metal, an electric charge is accumulated on a boundary of the semiconductor and the insulator at a voltage of a threshold voltage or higher, and the capacitance is increased as indicated by a profile **11***a* in FIG. 9D. When the ferroelectric substance is used to configure the inside of the memory element **6**, it is known that the C-V characteristic is shifted to right or left as indicated by profiles **11***b*, **11***c* in FIG. 9D because of a remanent polarization Pr which is generated if an electric field exceeding a coercive electric field is generated.

As described above, the memory element having the above-described structure has an asymmetric C-V characteristic. Therefore, an arrow is added to the terminal of the electrode to indicate the polarity of the memory element as shown in FIG. 9B.

| | | | | |
|---|---|---|---|---|
| 25 | 36 | 345/87-103.ccls. and ((reset$3 or chang$3 or vary$4) NEAR5 sampl$3 NEAR3 (tim$3 or clock)) | USPAT | 2003/12/04 19:41 |
| 26 | 33137 | (detect$3 or sens$3 or receiv$3 or input$5) WITH ( shift$5 or sampl$3) NEAR2 (tim$3 or clock$) | USPAT | 2003/12/04 19:45 |
| 27 | 1527 | 345/87-103.ccls. and "27" | USPAT | 2003/12/04 19:43 |
| 28 | 381 | 345/87-103.ccls. and ((detect$3 or sens$3 or receiv$3 or input$5) WITH ( shift$5 or sampl$3) NEAR2 (tim$3 or clock$)) | USPAT | 2003/12/04 19:43 |
| 29 | 361 | (345/87-103.ccls. and ((detect$3 or sens$3 or receiv$3 or input$5) WITH ( shift$5 or sampl$3) NEAR2 (tim$3 or clock$)) ) not (345/87-103.ccls. and ((reset$3 or chang$3 or vary$4) NEAR5 sampl$3 NEAR3 (tim$3 or clock))) | USPAT | 2003/12/04 19:43 |
| 30 | 3887 | (detect$3 or sens$3 or receiv$3 or input$5) WITH ( shift$5 or sampl$3) NEAR2 (tim$3 or clock$) NEAR3 (vary$3 or chang$3 or provid$3 or generat$3 or reset$5) | USPAT | 2003/12/04 19:45 |
| 31 | 48 | ((345/87-103.ccls. and ((detect$3 or sens$3 or receiv$3 or input$5) WITH ( shift$5 or sampl$3) NEAR2 (tim$3 or clock$)) ) not (345/87-103.ccls. and ((reset$3 or chang$3 or vary$4) NEAR5 sampl$3 NEAR3 (tim$3 or clock)))) and ((detect$3 or sens$3 or receiv$3 or input$5) WITH ( shift$5 or sampl$3) NEAR2 (tim$3 or clock$) NEAR3 (vary$3 or chang$3 or provid$3 or generat$3 or reset$5)) | USPAT | 2003/12/04 19:48 |

The above-described MFS structure will be described with the polarity reversed and connected in parallel. FIG. **10**B and FIG. **10**C are diagrams showing examples of the structure of the memory unit **30**. The C-V characteristics of the respective memory elements are assumed to be substantially the same. Remanent polarizations of the ferroelectric substances in the respective memory elements **6***a*, **6***b* are generated by applying an electric field exceeding a coercive electric field between the terminals **30***b* and **30***c*. When it is seen from the terminals **30***b* and **30***c*, the polarities of the memory elements **6***a*, **6***b* are in the same direction. By the generation of the remanent polarizations in the ferroelectric substances, the C-V characteristic of each memory element **6***a*, **6***b* is shifted, and its level is the same between the two memory elements **6***a*, **6***b*.

A terminal **30***d* will be described with the terminals **30***b*, **30***c* connected as shown in FIG. **10**C. At this time, when it is seen from the terminals **30***a* and **30***d*, the polarities of the memory elements **6***a*, **6***b* are in the opposite direction to each other.

FIG. **10**A is a diagram showing an example of the C-V characteristic of the memory unit **30**. The C-V characteristic between the terminals **30***a* and **30***d* is identical to a characteristic obtained when the C-V characteristics of the two memory terminals **6***a* and **6***b* are overlaid in an opposite direction. And, the C-V characteristic is symmetrical about the vertical axis (ground potential) as shown in FIG. **10**A. Besides, since the threshold voltages of the memory elements **6***a*, **6***b* vary by the same extent depending on the magnitude of a remanent polarization as indicated by a dotted line in the same drawing, the extension of the C-V curve varies without losing the symmetric form. Using the C-V characteristic shown in FIG. **10**A, the present invention controls the voltage to be applied to the liquid crystal layer **2**. When the memory unit **30** has a symmetrical C-V characteristic, only an AC voltage can be applied to the liquid crystal layer.

FIG. **9**A shows a series connection of the memory unit **30** and the liquid crystal layer **2** which have the parallel structure of the memory element **6** shown in FIG. **10**B and FIG. **10**C. In FIG. **9**A, a switch **10** is provided for making the description simple. This switch can be omitted.

To write a data signal as image information into the memory unit **30**, a predetermined voltage is applied between the terminals **30***b* and **30***c* with the switch **10** off. The applied voltage is determined to be at a level that an electric field exceeding a coercive electric field is generated in the ferroelectric substance in the memory elements **6***a*, **6***b* and a remanent polarization corresponding to the data signal is generated. When the memory elements **6***a*, **6***b* are designed to have the same structure, the remanent polarization to be generated is also same in the respective memory elements **6***a*, **6***b*.

Upon completing writing the data signal, the switch **10** is turned on, and the terminals **30***b*, **30***c* are controlled to have a ground potential. On the other hand, an AC voltage symmetrical about the ground potential is applied to the terminal **30***a*. The applied voltage is divided by the liquid crystal layer **2** and the memory elements **6***a*, **6***b*. At this time, it is designed not to generate an electric field exceeding a coercive electric field in the ferroelectric substances within the memory elements **6***a*, **6***b*. Since the parallel structure of the memory elements **6***a*, **6***b* has a C-V characteristic symmetrical about the ground potential, the voltage change of the terminal **30***e* is also symmetrical. As a result, the divided AC voltage is applied to the liquid crystal layer **2**. Since this voltage division is so effected that the DC component to be applied to the liquid crystal layer is excluded, the liquid crystal layer can be prevented from being deteriorated.

A point of symmetry of the C-V characteristic of the memory unit **30** is not required to be the ground potential. By displacing the voltage between the terminals **30***b*, **30***c* and the terminal **30***a* corresponding to the deviation from the ground potential, the AC voltage is applied to the liquid crystal layer **2**.

When the AC voltage can be applied to the liquid crystal layer **2**, it is quite effective against the liquid crystal from being deteriorated. If the voltage to be applied to the liquid crystal includes a DC component, degradation of the liquid crystal, called as image sticking, is caused due to the localization or the like of the electric charge on the liquid crystal orientation film or the like. But, in the present invention, since a perfect AC voltage can be applied to the liquid crystal layer **2**, the liquid crystal is not deteriorated at all, and a very reliable liquid crystal display device can be achieved. And, the capacitance which is variable with the pixel or time can be dealt with.

And, the liquid crystal display device of the present invention can control the voltage to be applied to the liquid crystal layer **2** in an analog fashion by varying the threshold voltages of the respective memory elements **6***a*, **6***b*. As the operation range of the memory elements **6***a*, **6***b*, by applying the data signal in a region where the C-V curve of the memory unit **30** varies gradually corresponding to the applied voltage and in the horizontal regions of the characteristic before and after the former region as shown in FIG. **10**A, the capacitances of the memory elements **6***a*, **6***b* vary corresponding to the threshold voltages of the memory elements **6***a*, **6***b*. As a result, the voltage to be applied to the liquid crystal layer **2** can be varied in an analog fashion without varying the voltage to be applied to the terminal **30***a*. Besides, since the symmetry of the C-V characteristic of the memory unit **30** which has the parallel structure of the memory elements **6***a*, **6***b* is retained, the DC voltage component is not applied to the liquid crystal layer **2**.

FIG. **12** is a diagram to describe a state of the ferroelectric substance in the memory elements **6***a*, **6***b* while the data signal is being written and the written data signal is being displayed. Description will be made with reference to the hysteresis curve of the ferroelectric substance.

To write the data signal into the memory unit **30** comprising the memory elements **6***a*, **6***b*, an electric field exceeding a coercive electric field Ec is applied to the ferroelectric substance, then the electric field is cleared to zero. Storage in the ferroelectric substance is made as a remanent polarization Pr corresponding to the data signal. If information had been stored in the ferroelectric substance, an electric field less than a coercive electric field −Ec is applied to the ferroelectric substance to clear the stored information, and an electric field of Ec or higher is applied to write new information. The magnitude of the remanent polarization Pr depends on the magnitude of the applied voltage.

On the other hand, in the image displayed state, the generation of an electric field in the ferroelectric substance within the memory elements **6***a*, **6***b* is less than the coercive electric field. Therefore, the remanent polarization Pr does not vary and its operation is limited to the range shown in FIG. **12**. The invention uses the magnitude of the remanent polarization Pr to control gradation. Since the remanent polarization Pr is quite stably held by the ferroelectric substance, memory for the data signal of halftone is outstanding.